



Procedures and Guidelines (PG)

DIRECTIVE NO. 500-PG-8700.2.2C
EFFECTIVE DATE: 08/10/10
EXPIRATION DATE: 02/10/16

APPROVED BY Signature: Original signed by:
NAME: Dennis Andrucyk
TITLE: Director of AETD

COMPLIANCE IS MANDATORY

Responsible Office: 500 /Applied Engineering and Technology Directorate

Title: Electronics Design and Development

PREFACE

P.1 PURPOSE

This PG establishes guidelines for the Product Design Team (PDT) members providing electronics design and development support to GSFC products covered by the scope of the GSFC Quality Management System.

P.2 APPLICABILITY

This procedure applies to the electronics design and development of all Goddard Space Flight Center (GSFC) products and processes covered by the scope of the GSFC Quality Management System.

P.3 AUTHORITY

GPR 1280.1, The GSFC Quality Manual
GPR 8700.1, Design Planning and Interface Management
GPR 8700.2, Design Development

P.4 REFERENCES

GPR 1310.1, Customer Commitments and Review
GPR 1410.2, Configuration Management
GPR 1710.1, Corrective and Preventive Action
GPR 5330.1, Product Processing, Inspection, and Test
GPR 5340.2, Control of Nonconformances
GPR 8700.3, Design Validation
GPR 8700.4, Integrated Independent Reviews (IIRs)
GPR 8700.6, Engineering Peer Reviews
500-PG-8700.2.5, Engineering Drawing Requirements Manual
500-PG-8700.2.7, Design of Space Flight Field Programmable Gate Arrays
500-PG-8700.2.8, Field Programmable Gate Array Development Methodology
547-PG-8072.1.1, Manufacturing Process

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EEE-INST-002, Instructions for EEE Parts Selection, Screening, Qualification and Derating
 GSFC Form 4-30, Work Order Authorization and Continuation Sheet
 GSFC-CM-001, GSFC Configuration Management Manual
 GSFC-WM-001, Electrostatic Discharge Workmanship Manual
 GSFC-STD-1000, Rules for the Design, Development, Verification, and Operation of Flight Systems
 Form 547 – WR, Advanced Manufacturing Branch Work Request

P.5 CANCELLATION

500-PG-8700.2.2 Rev B, Electronics Design and Development Guidelines

P.6 SAFETY

NONE

P.7 TRAINING

NONE

P.8 RECORDS

Record Title	Record Custodian	Retention
Design Planning Documentation Reference: GPR 8700.1	Product Design Lead (PDL)	NASA Records Retention Schedule (NRRS) 8/103. Engineering test and evaluation data. Temporary. Destroy between 5 and 30 years after program/project termination.
Work Order Authorization (WOA), completed Reference: PG 5330.1 GSFC Form 4-30	Product Manager (PM)	NRRS 8/103.
Integrated Independent Review Team (IIRT) Reports including RFA's: Project responses to RFA's; IIRT decisions on project responses Reference: PG 8700.6	Product Manager	NRRS 8/101. Permanent. Cut off records at close of program/project or in 3-year blocks for long term programs/projects. Transfer to Federal Records Center (FRC) after cutoff. Transfer to National Archives and Records Administration (NARA) 7 years

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		after cutoff.
Engineering Peer Review (EPR) Report including RFA's, RFA Responses, RFA Originator Decisions, Summary Status of RFA's	PDL using project's Configuration Management (CM) System	NRRS 8/103.

* *NRRS – NASA Records Retention Schedule ([NPR 1441.1](#))*

P.9 MEASUREMENT/VERIFICATION

The Responsible Office for this procedure shall ensure that internal and external third party audit findings related to effective design development are used to assess the procedure's effectiveness.

PROCEDURES

In this document, a requirement is identified by "shall," a good practice by "should," permission by "may" or "can," expectation by "will," and descriptive material by "is."

The PDL is responsible for the quality and timely completion of the electronics design and development activities as specified in the Customer Commitments and Review, GPR 1310.1, and/or Statements of Work (SOW). This includes providing the design output (documentation including engineering drawings, test plans, procedures, and reports), budgets, schedules, and review support to the customer (typically a project or instrument manager). It is the responsibility of the PDL, in partnership with the customer, to determine and document in a design plan (per GPR 8700.1, Design Planning and Interface Management) which specific steps of the typical electronics design and development process will be executed.

1. Compilation of Design Inputs

The PDL shall compile and evaluate the Design Inputs, which may include one or more of the following:

- a. Statement of Work
- b. Customer-imposed requirements
- c. Interface Control Drawings (ICDs)
- d. Applicable NASA directives, internal requirements, specifications, standards, and statutory/regulatory requirements
- e. Applied Engineering and Technology Directorate (AETD) imposed requirements

2. Initial Planning

2.1. The PDL develops the design planning documentation, which contains a high level description of the electronics hardware to be developed, key support personnel, a budget, and a schedule for review and approval by the customer. The plan should include adequate contingencies for completion of the design and development activity within the resources negotiated in the Customer Agreement and/or SOW (see GPR 1310.1, Customer Commitments and Review). A project or instrument manager may request this design plan information be documented in a formal Implementation Plan for the electronics subsystem. Other approaches may be to have the design planning documents combined with other discipline inputs and consolidated into a Project Plan. Alternatively the design planning documentation may be part of several individual project documents. Regardless of the approach, the design planning documentation is a quality record and shall be maintained per the applicable configuration management plan for this design and development activity.

2.2. The PDL ensures that the PDT is composed of individuals, civil servants and/or contractors as necessary, with the required discipline skills.

3. Requirements Definition

The PDL supports the generation of a requirements document from design inputs. It may be necessary for the PDT to perform various analyses in order to derive lower level design requirements from the top-level design inputs. These top level and derived requirements shall be documented, reviewed for adequacy and consistency with relevant NASA and GSFC standards, and signed off by the PDL and the customer. The requirements documents shall be maintained per the applicable configuration management plan.

4. Design Practice

The design effort should be conducted according to the following good design practices, as appropriate:

- 4.1 Multiple design concepts should be identified, and the best selected by a trade study process. The best design concept is that which fully meets all of the design requirements and considers cost, technical complexity, schedule, risk, technology infusion, design heritage, and other factors as appropriate. It may be necessary to prototype one or more of the design options and to conduct various performance and/or environmental tests before the optimum design path is chosen. In any case, the customer may be a key participant in this critical concept selection process, as needed. In addition, the results of the trade study process are typically “peer reviewed” (see GPR 8700.6, Engineering Peer Reviews).
- 4.2 The PDL should query the NASA Engineering Network Lessons Learned (ENLL) website (<http://nen.nasa.gov/portal/site/llis/LL>). The NASA ENLL is an on-line, automated database system designed to collect and make available for use the NASA lessons learned from many years in the aeronautics and space business. The ENLL enables the knowledge gained from past experience to be applied to current and future projects. Its intent is to avoid the repetition of past failures and mishaps, as well as the ability to share observations and best practices. Through this resource, the PDL may facilitate the early incorporation of safety, reliability, maintainability, and quality into the design of flight and ground support hardware, software, facilities, and procedures.
- 4.3 Designs shall be developed in accordance with the fundamental design principles and requirements described in the Design, Development, Verification, and Operation of Flight Systems (GSFC-STD-1000), also known as the Gold Rules. Any deviation must be approved by project waiver or exception.
- 4.4 Detailed designs should be as simple as possible, making maximum use of standardization, repeated elements, known processes, and readily available military and space qualified parts and materials.

All parts included in the design shall meet the part quality level requirements as established by project requirements and the Instructions for Electrical, Electronic and Electromechanical (EEE) Parts Selection, Screening, Qualification and Derating (EEE-INST-002). A documented Parts Control Program shall be implemented to select, control, and approve all parts in the design.
- 4.5 Designs should be robust and use parts and materials capable of meeting the performance and reliability requirements in typical and/or expected environmental conditions (e.g. radiation environment, thermal variations, etc.)
- 4.6 All appropriate functional discipline personnel (e.g. manufacturing, testing, thermal and other subsystems), who are involved in or associated with the system or item under design, should

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be included in the PDT, or as a minimum, be consulted to review the design and make suggestions to improve manufacturability, testability, and/or reduce the costs associated with such activities. The PDL shall decide whether to accept or reject the recommendations.

- 4.7 Final product designs shall be documented using standard GSFC electronics drawing practices (see 500-PG-8700.2.5, Engineering Drawing Requirements Manual). Typical product documentation sets include electronic schematics, wiring diagrams, drill drawings, parts lists, and assembly drawings. Instructions for obtaining official GSFC drawing numbers can be found in GSFC-CM-001, GSFC Configuration Management Manual as referenced in GPR 1410.2, Configuration Management. The drawing practices in 500-PG-8700.2.5, Engineering Drawing Requirements Manual, may be applicable to pre-flight and pre-operational hardware (e.g. engineering test units, breadboards, and proof-of-concept hardware), but are not required. The PDL shall determine the applicability.
- 4.8 The design of systems using custom microelectronic devices such as application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA) is a part of current engineering practice. Such designs shall be performed in accordance with the 500-PG-8700.2.7, Design of Space Flight Field Programmable Gate Arrays and 500-PG-8700.2.8, Field Programmable Gate Array Development Methodology.
- 4.9 The following checklist of electronic design considerations is provided as an aid in generating and implementing the design:
- a. application (space flight, ground, aircraft, balloon, sounding rocket, etc.)
 - b. critical functions
 - c. timing margins
 - d. resource margins (mass, power, volume, FPGA/central processing unit (CPU) usage)
 - e. environmental conditions (thermal, radiation, vibration, etc)
 - f. power/thermal dissipation
 - g. electro-magnetic interference (EMI), electro-magnetic compatibility (EMC)
 - h. parts quality requirements and parts control program
 - i. parts application in design (e.g. radiation, life considerations)
 - j. electrostatic discharge (ESD) sensitivity level
 - k. packaging strategy
 - l. testability
 - m. ground support equipment
 - n. flight software compatibility

5. Design Changes

Design changes, as required by customer request, process improvement, errors in the original design, improper component selection, drawing error, product non-conformances, etc., shall be documented, approved, and implemented per the relevant configuration management plan.

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6. Design Reviews

At appropriate stages throughout the electronics design and development process, reviews shall be scheduled and conducted.

6.1 Internal reviews are held during the design process and are truly at the grass roots level.

Participants of these informal reviews are usually members of the PDT and other electronics engineers (external to the team). Though not required, informal documentation and tracking of action items sometimes occurs at the discretion of the PDL.

6.2 Peer Reviews (see GPR 8700.6, Engineering Peer Reviews) are more formal reviews that evaluate a design's technical status using a team of appropriate specialists independent of the Product Design Team. They are conducted as specified in the Engineering Peer Review Plan. Emphasis is placed on selecting a well-rounded review team consisting of personnel cognizant of and experienced with the subject matter of the review. These reviews are conducted to ensure that the electronics design meets the design requirements. It is the responsibility of the PDL and/or the PDT to respond to all Requests For Action (RFAs) generated at the reviews. The method for RFA tracking and closure will be established through communication with the customer. Engineering Peer Reviews can be scheduled at any time during the design and development process. Some typical reasons for scheduling an Engineering Peer Review could be any one or more of the following:

- a. Required per the Engineering Peer Review Plan
- b. Review a new design
- c. Review results of a trade study
- d. Review modifications to an existing design or to existing design requirements
- e. Preparation for an Integrated Independent Review
- f. Preparation for a complex functional or environmental test
- g. Preparation for a complex shipment of hardware

6.3 Integrated Independent Reviews (see GPR 8700.4, Integrated Independent Reviews) provide expert technical review of the end-to-end mission system and are conducted at the system-level at critical milestones in project formulation and implementation. They are conducted as specified in the project's Integrated Independent Review Plan. The status of the electronics design and development is presented at these reviews by the electronics PDL/PDT. Other PDLs/PDT members present the status of their respective subsystems at these reviews. These reviews are conducted to ensure that the system design fully meets the design requirements. Again, it is the responsibility of the PDL and/or PDT to respond to all RFAs generated at the reviews for their respective subsystem. Reviews typically conducted include a Systems Concept Review, Preliminary Design Review, Critical Design Review, Pre-Environmental Test Review, and a Pre-Ship Review.

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7. Design Verification

During the engineering design and development process, design verification will be conducted as required to ensure that the design meets the customer's requirements. Verification will be conducted by a combination of analysis, review, and test.

7.1 The following analyses will be performed and documented as appropriate:

- a. Various circuit analyses (simulation, timing, EMC, parts stress, signal integrity, worst case circuit, fixed point/floating point, etc)
- b. Circuit, board, or box-level thermal and/or structural analysis
- c. Printed Wiring Board (PWB) coupon analysis
- d. Review and comparison to similar systems/designs

7.2 Engineering Peer Reviews and Integrated Independent reviews will be conducted as described in Section 6 of this procedure to verify that the design and test documentation meets all customer requirements.

7.3 Development and testing of proof-of-concept designs, breadboards, engineering test units, and/or life test units may also be conducted as part of the design verification.

7.4 The Work Order Authorization (WOA) shall be utilized (see GPR 5330.1, Product Processing, Inspection, and Test) to plan and document the processing of a product as it progresses from the initial stages of manufacture through integration, inspection, and test events, including all functional and environmental test, required for design verification.

7.5 Test results shall be evaluated to ensure that design requirements have been verified. Anomalies found during the verification process shall be documented and resolved per project and/or organizational requirements, usually per GPR 5340.2, Control of Nonconformances, and GPR 1710.1, Corrective and Preventive Action.

8. Product Validation

The PDL/PDT shall validate the product in accordance with GPR 8700.3, Design Validation. Validation includes manufacture, integration to larger systems/assemblies, as well as environmental and functional tests. Note that due to the iterative nature of the design process, intermediate validation is frequently required.

8.1 The PDL shall determine the most appropriate and efficient method for the fabrication of mechanical hardware. Options include the Code 547 Machine Shop, which provides a full complement of planning, contracting, and monitoring services (see 547-PG-8072.1.1, Manufacturing Process), in-house manpower, task order contracts, or any other contracting medium that accesses a viable fabrication resource. Please note that fabrication tasks processed through Code 547 require a Work Request (Form 547-WR) to

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initiate the fabrication effort, and do not require a WOA. The PDL is responsible for identifying the critical dimensions and for the disposition of any discrepancies.

8.2 All ground support equipment (GSE) and test equipment that interfaces with flight hardware must be subject to the considerations listed below. It will be the responsibility of the PDL to ascertain that:

- a. All GSE is properly calibrated and certified
- b. A test procedure exists and is followed for the performance of all tests
- c. All interfaces between the GSE and the flight hardware are clearly documented in an interface control document (ICD)
- d. Any modifications to the GSE shall be reviewed by a Peer Review Team for completeness, correctness, and proper documentation before the GSE can be used again with the flight hardware
- e. A Safe-To-Mate test between the GSE and the flight hardware must be conducted and documented the first time the two are connected together and every time a modification affecting the interface is made to either item
- f. A clear and complete test setup configuration diagram exists and is readily available
- g. Verification is made that the physical test setup conforms to the test setup configuration diagram before the performance of each test. This verification must be documented as the first step in all subsequent test procedures.
- h. Discrepant parts may be dispositioned as “rework”, repair, use-as-is, reclassify, return to vendor, or scrap. See GPR 5340.2, Control of Nonconformances.

8.3 Assembly and integration of space flight electronics hardware shall be performed in accordance with an assembly drawing and/or plan. Integration, inspection, and test events shall be documented via the WOA process defined in GPR 5330.1, Product Processing, Inspection and Test. All assembly and integration activities shall be performed with the appropriate safety considerations addressed for personnel and/or hardware, and under the appropriate environmental conditions. Some items for consideration are:

- a. Cleanliness requirements
- b. Temperature/Humidity requirements
- c. ESD control (See GSFC-WM-001)
- d. Adequate space
- e. Unique power and/or grounding requirements
- f. Alignment operations requiring GSE
- g. EMI/EMC (Cell Phones can negatively affect certain electronic systems)

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8.4 Validation testing shall be conducted using approved (CM released) validation test plans and procedures. The following list of validation test, the majority of which have significant electronic design implications, shall be conducted as appropriate:

- a. Interface Testing (mechanical and electrical)
- b. Functional Testing
- c. Life Testing
- d. Vibration Testing
- e. Acoustics Testing
- f. Ambient Pressure Thermal Testing
- g. Thermal/Vacuum Testing
- h. Thermal Balance Testing
- i. EMI/EMC Testing
- j. Magnetic Testing

8.5 All tests shall be analyzed and evaluated to ensure that all customer requirements have been validated. Anomalies found during the validation process shall be documented and resolved per GPR 5340.2, Control of Nonconformances, and GPR 1710.1, Corrective and Preventive Action.

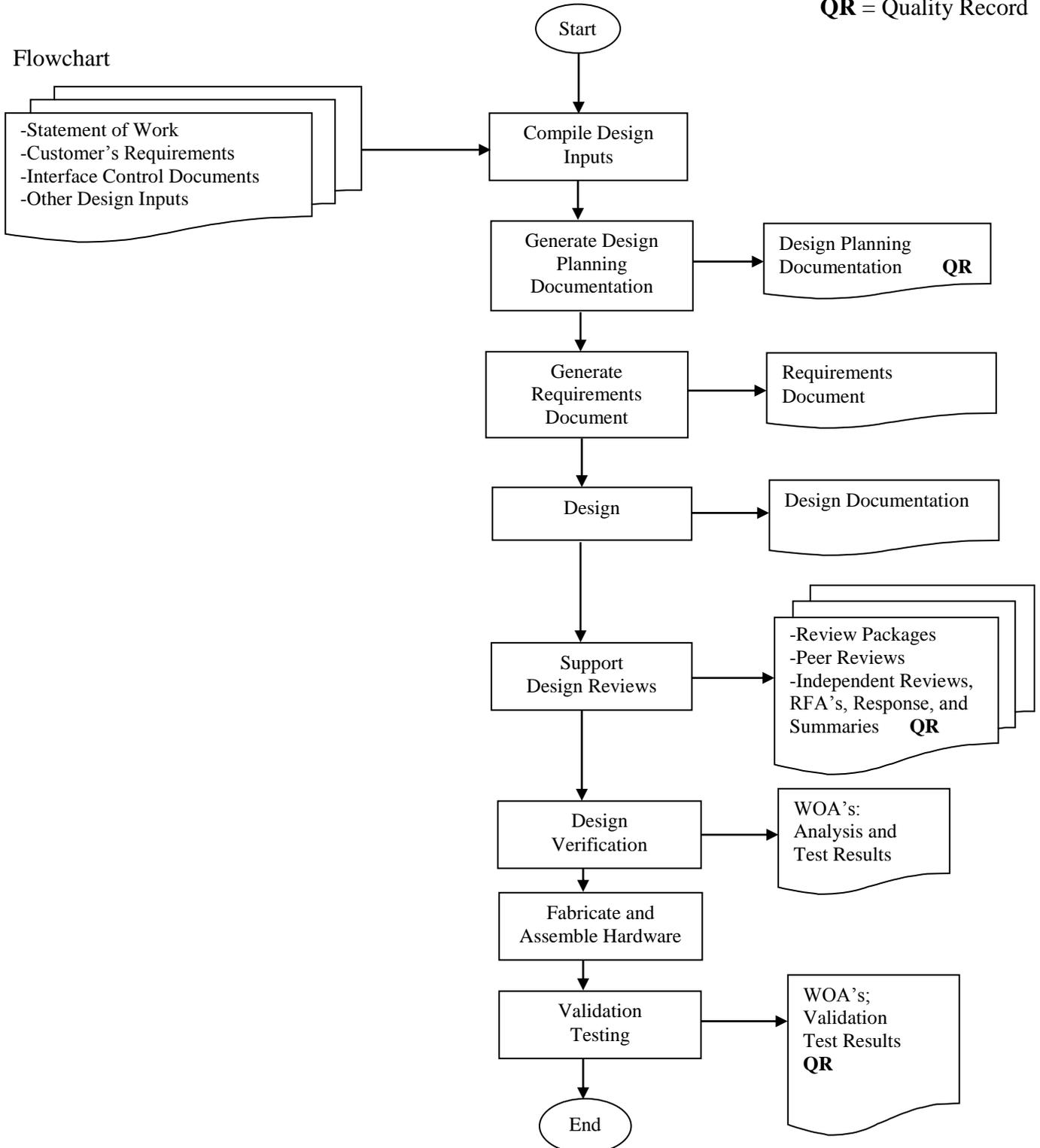
9. Communicate Design Output

The PDL/PDT shall assure that both the design output (e.g. engineering drawings, electronic models, test plans, procedures, reports, review documentation) and the design progress (technical, budget, schedule) are communicated to the appropriate configuration management system (see GPR 1410.2, Configuration Management) and to the customer upon request.

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All steps are the responsibility of the PDL and/or PDT.
QR = Quality Record

Flowchart



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Appendix A – Definitions

1. Product Design Lead is the manager or leader that is responsible for managing the design activity, managing the technical and organizational interfaces identified during the design planning, and where required, forming and leading the PDT. The term PDL may refer to flight project managers, mission managers or others who have the responsibility for managing a design activity.
2. Customer – Any organization or person receiving electronics design and development support from the AETD.
3. Design Plan – The documentation created as a result of executing PG 8700.1, Design Planning and Interface Management. This document consists of schedules, budgets, a work breakdown structure (WBS), a verification plan, and other information. It may be gathered together as a single document, consist of multiple documents, or be a portion of a more comprehensive document such as a Project Plan, or equivalent.
4. Interface Control Document – A specification of the mechanical, thermal, electrical, power, command, data, and other interfaces that system elements must meet.
5. Verification – Proof that the design is compliant with requirements and specifications. May be determined by test, analysis, and inspection.
6. Validation – Proof that the product accomplishes the intended purpose. May be determined by test, analysis, and demonstration.

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Appendix B – Acronyms

AETD – Applied Engineering Technical Directorate
ASIC – Application Specific Integrated Circuits
CM – Configuration Management
CPU – Central Processing Unit
EEE – Electrical, Electronic, and Electromechanical
EMC – Electromagnetic Compatibility
EMI – Electromagnetic Interference
ENLL – Engineering Network Lessons Learned
EPR – Engineering Peer Review
ESD – Electrostatic Discharge
FPGA – Field Programmable Gate Array
FRC – Federal Records Center
GPR – Goddard Procedural Requirements
GSE – Ground Support Equipment
GSFC – Goddard Space Flight Center
ICD – Interface Control Drawing
IIRT – Integrated Independent Review Team
NARA – National Archives and Records Administration
NRRS – NASA Records Retention Schedule
PDL – Product Design Lead
PDT – Product Design Team
PWB – Printed Wiring Board
RFA – Request For Action
SOW – Statement Of Work
WBS – Work Breakdown Structure
WOA – Work Order Authorization

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
Baseline	01/14/1999	Initial Release
A	07/02/1999	Modified format to conform to GPG 1410.1. Corrected incorrect document numbers in references. Listed references in numerical order. Clarified quality records requirements in text and flow chart. Clarified WOA usage requirements for verification and validation. Clarified drawing standards requirements for engineering test units versus flight units.
B	02/01/2005	Modified format to conform to GPG 1410.1. Corrected multiple reference documents throughout this PG to reflect current titles and/or document numbers. Clarified Integrated Independent Reviews (see section 6.3). Included new reference to instructions for use of EEE parts (see section 4.3). Include new reference to ASIC and FPGA design (see section 4.7).
C	08/10/10	Modified format to conform to GPR 1410.1. Corrected incorrect document numbers, updated the references section. Removed "Guidelines" from title. Added several items to Definition section. Updated Section 4.2 to reference ENLL. Added technical clarification and refinements to many paragraphs in the Procedures section.
	07/08/15	Administratively extended for six months.

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